Notice of Allowability	Application No.	Applicant(s)	
	10/017,160	LI ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed April 4, 2006*.

2. ☒ The allowed claim(s) is/are *1-13, 15, 18-27, 29-32, 34, 35, 37-57 renumbered as claims 1-51*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060609*.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. Claims 1-13, 15, 18-27, 29-32, 34, 35, 37-57 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Anthony B. Diepenbrock on June 9, 2006.

The application has been amended as follows wherein the following versions of claims 1, 3-5, 11, 20, 31, 39, 52 and 57 replace all prior versions in their entirety:

1. A circuit for jitter measurement, comprising:

a plurality of delay elements arranged in a series-connected chain having a total delay equal to [the]a sum of [the]each delay[s] of the delay elements, each delay element having an input and output, wherein the input of the first element in the chain [has an input that] receives an input clock signal, the chain propagating the input clock signal through each of its delay elements, and each delay element output producing a delayed version of the propagated input clock signal on its input;

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; [and]

a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay [which] that is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in the corresponding storage

elements one or more pulses that may be active at the time of occurrence of the trigger signal[, wherein the second set of circuitry further includes]; and

a single one detector operative to select one from the recorded pulses in the storage elements at the time of occurrence of the trigger signal, [and]wherein a jitter measurement is made based on the selected pulses after a plurality of trigger signals has occurred.

3. The circuit of claim 1, wherein there is a number N of elements in the plurality of delay elements and [wherein the number of delay elements in the chain is N, where] N is an even number greater than 2 and implemented as a power of 2.

4. The circuit of claim 1, wherein the [associated] delay of each delay element is controlled by a delay control circuit.

5. The circuit of claim 4,

wherein the delay of at least one of the plurality of [associated]delay[s] elements is not equal to the delay of any other of the plurality of [associated] delay[s] elements, and

wherein the delay control circuit is a charge pump controlled delay lock loop.

11. The circuit of claim 1, wherein the second set of circuitry includes a first plurality of latching circuits, each one of the first plurality of latching circuits corresponding to one of the plurality of delay elements.

20. The circuit of claim 19, wherein the third set of circuitry includes a second plurality of latching circuits each, each one of the second plurality of latching circuits corresponding to one of the plurality of delay elements.

31. A method for measuring jitter of a clock signal, comprising:

for each of a plurality of trigger signal occurrences, performing the steps of:

receiving the clock signal, the clock signal having a significant instant;

propagating the significant instant of the clock signal through a chain of delay elements, wherein each element of the chain has an associated delay and the chain has a total delay equal to the sum of the associated delays;

receiving a trigger signal and delaying the received trigger signal so as to occur at a time equal to approximately half the total delay of the chain;

detecting the propagation of the significant instant of the clock signal through each of the delay elements in the chain and producing a pulse corresponding [thereto]to each of the delay elements;

if multiple pulses are produced coincident with the trigger signal, filtering the multiple pulses to provide one filtered pulse coincident with the trigger signal; and

recording the filtered pulse that is coincident with the trigger signal; and

producing a jitter measurement signal responsive to ~~the~~ a plurality of filtered pulses after the plurality of trigger signal occurrences.

39. The method of claim 31, wherein the filtering step further comprises determining a difference between an earliest and a latest occurrence in the chain of the propagating significant instant.

52. The system of claim 46, wherein the output of one of the plurality of delay elements is connected to the input of a [the] next adjacent one of the plurality of delay elements.

57. A jitter measurement circuit comprising:

a plurality of delay elements arranged in a series-connected chain having a total delay equal to [the] a sum of [the] each delay[s] of the delay elements, each having an input and an output, wherein the input of the first element in the chain [has an input that] receives an input clock signal, the chain propagating the input clock signal through each of its delay elements, and each delay element output producing a delayed version of the propagated input clock signal on its input;

a first set of circuitry operative to produce at an output a pulse corresponding to each delay element in response to the propagation of a significant instant of the input clock signal through the delay element, each pulse having a width that is approximately equal to the delay of the corresponding delay element; and

a second set of circuitry having one storage element corresponding to each output of the first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a delay [which] that is approximately half of the total delay of the chain, and the second set of circuitry being operative to record in each[the] corresponding storage element any pulse that is active at the time of occurrence of the trigger signal[, wherein a jitter measurement is made based on the pulses recorded in the storage elements after a plurality of trigger signals has occurred];

a single one detector operative to select one from the recorded pulses in the storage elements at the time of occurrence of the trigger signal [for receiving a reset signal and

for filtering the measure of jitter by selecting one instance of the recorded pulses in response to occurrence of the reset signal];

multiple event recorder circuitry operative to capture the selected one of the recorded pulses in the single one detector upon occurrence of each of a plurality of trigger signals, wherein a jitter measurement is made based upon the captured selected pulses; and

a result calculator for producing statistical information about occurrences in the chain of the significant instance of the input clock signal.

Claims 1-13, 15, 18-27, 29-32, 34, 35, 37-57 are renumbered as claims 1-51, respectively, and the claim dependency is renumbered accordingly.

Allowable Subject Matter

3. Claims 1-13, 15, 18-27, 29-32, 34, 35, 37-57 renumbered as claims 1-51 are allowed.

4. The following is an examiner's statement of reasons for allowance:

Claims 1-13, 15, 18-27, 29-32, 34, 35, 37-57 renumbered as claims 1-51 are allowed because the prior art of record does not disclose or obviate a system for responding to jitter comprising a jitter measurement apparatus with a single one detector or method wherein a delay line is used to capture an input signal edge for the measurement of the jitter and further utilizing and the jitter measurement to adjust a parameter of the system adaptively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason M. Perilla

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER